Testing VTX Module1 with NCC Electronics

Strange pedestals of J2 half when reading all sensor (12 chips)

Reading halves of the sensor shows much better pedestals.
Note, in this setup, the receiving data connectors are ganged together. On the VTX FEE they are read out separately

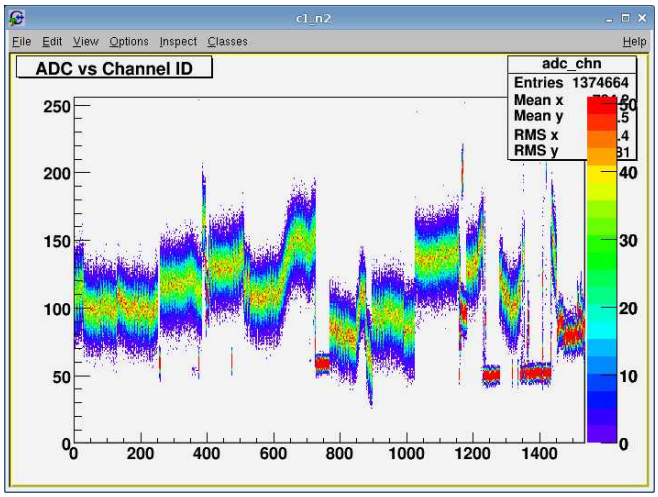

Fig. 1: HV=20V

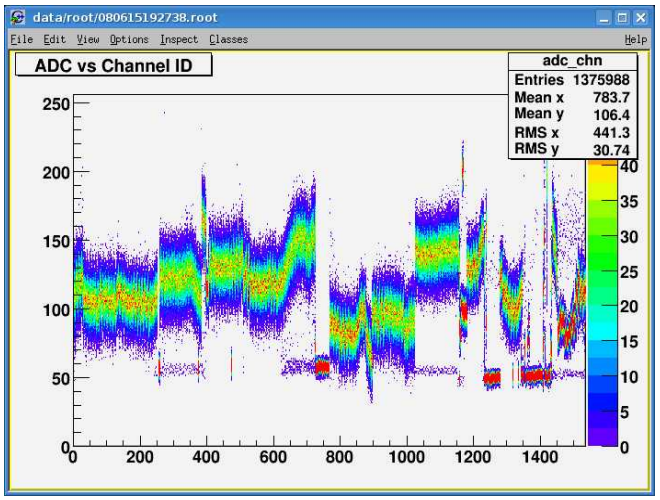

Fig. 2: HV=100V, 1200nA

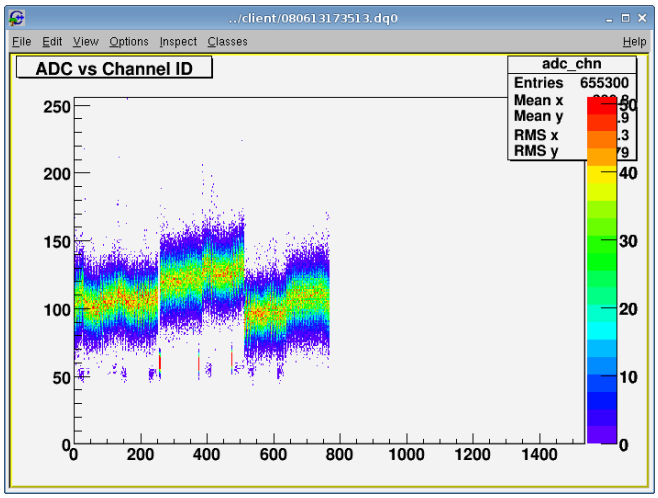

Fig. 3: Half-sensor J1, HV=100, J2 disconnected.

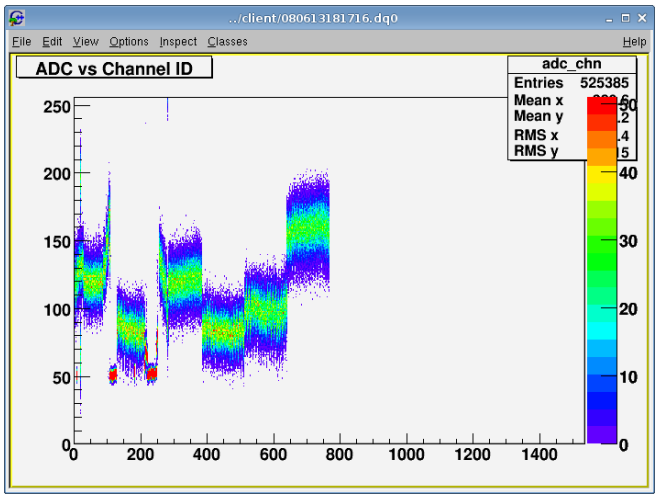

Fig. 4: Half-sensor J2 is connected to Y connector, HV 20V.

Masking out all channels on one half of the module affects pedestals on the other half.

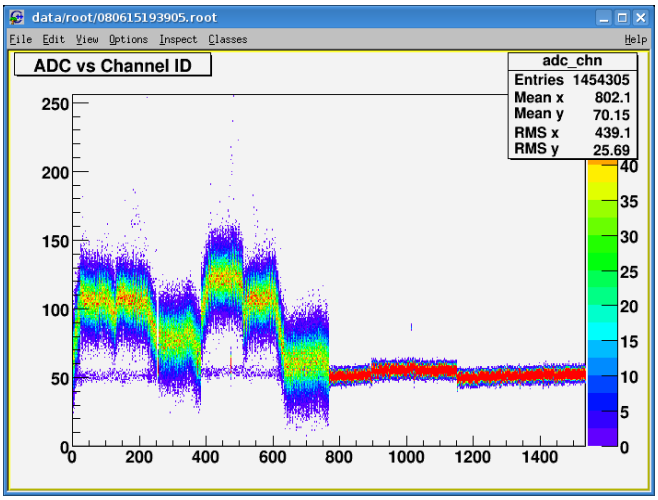

Fig. 5: HV=100V, preamps of J2 half are disabled

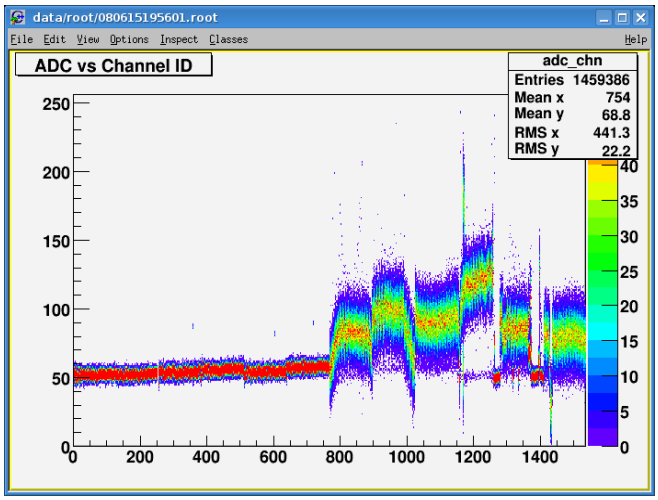

Fig. 6: HV=100V, preamps of J2 half are disabled.

AGND and DGND are disconnected on the crossboard.

In all other runs the AGND was connected to DGND on the crossboard. The AGND and DGND are provided from a dual power supply, they are isolated.

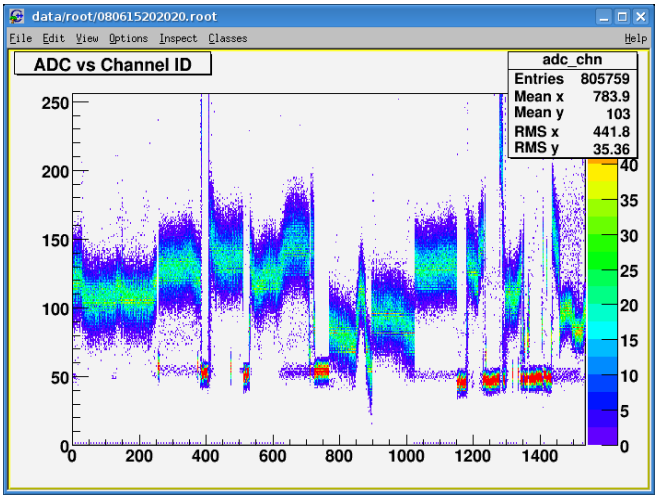

Fig. 7: HV=100V. AGND disconnected from DGND on the crossboard.

Changing AVDD and DVDD from 2.5 to 2.6V

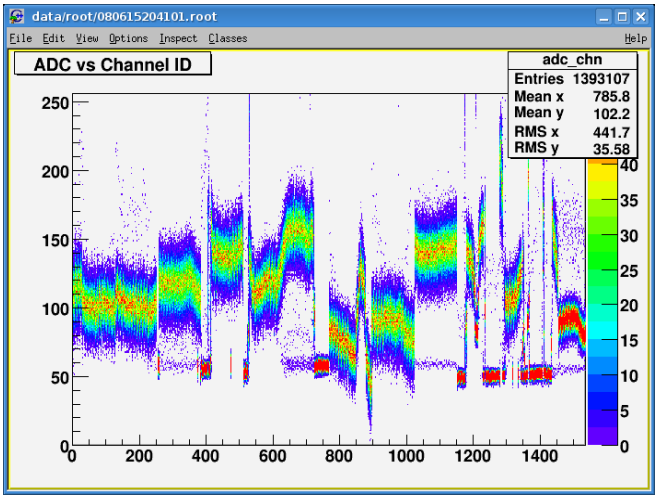

Fig. 8: HV=100V, AVDD changed from 2.5 to 2.6V, current = 0.615A, DVDD = 2.5V, 0.313A.

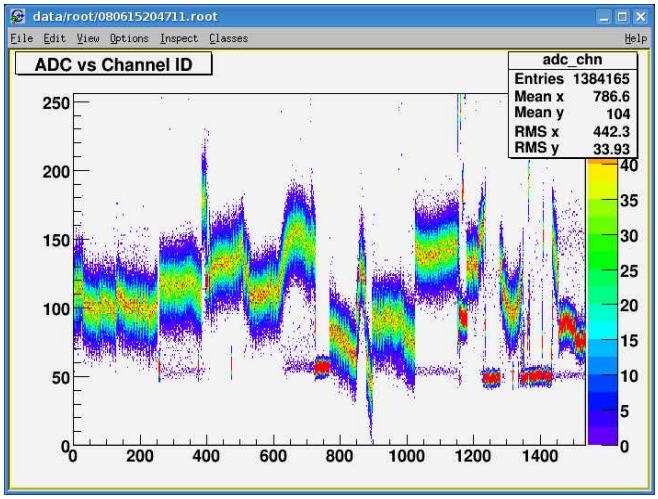

Fig. 9: HV=100V, DVDD changed from 2.5 to 2.6V, currents: DVDD = 0.333, AVDD= 2.6V, 0.637A

Calibration pulses disabled, pedestals changed drastically.

In all previous runs the calibration pulse 0.8V (VCAL=1) was applied to every 8th channel.

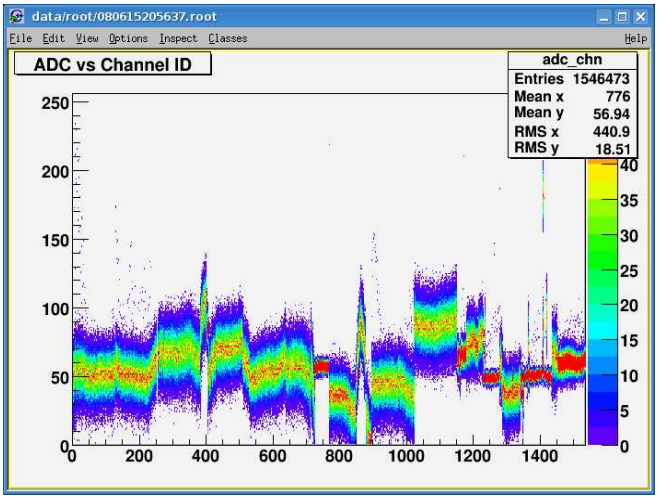

Fig. 10: HV = 100V, all Cal pulses are disabled, previously the Cal pulses were applied to every 8th channel.